What is claimed is:

1. A method of fabricating an integrated circuit on a wafer, the method comprising:

forming a gate electrode stack over a gate dielectric;

forming nitride spacers along sidewalls of the gate electrode stack other than along lowermost portions of the sidewalls; and

subsequently performing a reoxidation process with respect to the gate dielectric..

2. The method of claim 1 further including:

forming an oxide layer adjacent the lowermost portions of the sidewalls prior to forming the nitride spacers.

3. The method of claim 2 wherein the oxide layer is formed using a high density plasma process.

4. The method of claim 2 wherein the oxide layer is formed using a collimated sputtering process.

5. The method of claim 2 wherein the oxide layer is formed using a flowfill technique.

6. The method of claim 2 further including removing portions of the oxide layer to expose upper portions of the sidewalls prior to forming the nitride spacers.

7. The method of claim 2 wherein the oxide layer is formed using a process that results in a thicker

oxide being formed on horizontal surfaces of the wafer than along the sidewalls of the gate electrode stack.

8. The method of claim 7 wherein, following the act of forming the nitride spacers, at least a portion of the oxide formed on the horizontal surfaces is removed prior to performing the reoxidation.

9. The method of claim 7 wherein the oxide is removed from the horizontal surfaces using a selective wet etch.

10. The method of claim 7 wherein substantially all the oxide is removed from the horizontal surfaces prior to performing the reoxidation.

11. The method of claim 2 wherein forming nitride spacers includes:

forming a nitride layer over the wafer; and

etching the nitride layer to form the nitride spacers.

12. The method of claim 11 wherein forming a nitride layer includes depositing a nitride layer by chemical vapor deposition.

13. The method of claim 11 wherein etching the nitride layer includes performing an anisotropic etch.

14. The method of claim 11 wherein etching the nitride layer includes performing a reactive ion etch process.

15. A method of fabricating an integrated circuit on a wafer, the method comprising:

forming a word line stack over a gate dielectric, wherein forming the word line stack includes forming a polysilicon layer on the gate dielectric and forming a metal layer above the polysilicon layer;

forming nitride spacers along portions of sidewalls of the word line stack adjacent the metal layer, wherein at least lower portions of sidewalls of the polysilicon layer are not covered by the nitride spacers; and

subsequently performing a reoxidation process.

16. The method of claim 15 wherein forming a word line stack further includes forming a barrier layer above the polysilicon layer, and wherein forming nitride spacers includes forming nitride spacers along portions of the sidewalls of the word line stack adjacent the barrier layer.

17. The method of claim 15 further including:

forming an oxide layer over the wafer prior to forming the nitride spacers, wherein the oxide layer is thicker on substantially horizontal surfaces than along substantially vertical surfaces.

18. The method of claim 16 wherein the oxide layer is at least about four times thicker on the substantially horizontal surfaces than along the substantially vertical surfaces.

19. The method of claim 16 wherein the oxide layer is at least about ten times thicker on the

substantially horizontal surfaces than along the substantially vertical surfaces.

20. The method of claim 16 wherein the oxide layer is formed using a high density plasma process.

21. The method of claim 16 wherein the oxide layer is formed using a collimated sputtering process.

22. The method of claim 16 wherein the oxide layer is formed using a flowfill technique.

23. The method of claim 16 further including removing portions of the oxide layer to expose the portions of the sidewalls adjacent the metal layer prior to forming the nitride spacers.

24. A method of fabricating an integrated circuit on a wafer, the method comprising:

sequentially forming a polysilicon layer, a conductive barrier layer, and a metal layer over a gate dielectric formed on the wafer;

etching the polysilicon, conductive barrier and metal layers to form at least one gate electrode stack;

forming an oxide layer adjacent lower portions of sidewalls of the polysilicon layer;

providing nitride spacers along sidewalls of the conductive barrier and metal layers; and

performing a reoxidation process with the nitride spacers serving as a barrier to prevent an oxidizing species from interacting with the metal layer and the barrier layer.

Exhibit B'

25. An integrated circuit comprising:

a semiconductor wafer;

a gate dielectric film disposed on a surface of the wafer;

a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers; and

nitride spacers extending along sidewalls of the gate electrode stack other than along lowermost portions of the sidewalls.

26. The integrated circuit of claim 25 wherein the stack includes a polysilicon layer on the gate dielectric film and a metal layer above the polysilicon layer, and wherein the spacers extend along sidewalls of the metal layer.

27. The integrated circuit of claim 26 wherein the metal layer comprises a material selected from a group consisting of a refractory metal or a refractory metal alloy.

28. The integrated circuit of claim 26 wherein the stack includes a conductive barrier layer between the polysilicon layer and the metal layer, and wherein the spacers extend along sidewalls of the barrier layer.

29. The integrated circuit of claim 28 wherein the barrier layer is substantially impermeable to silicon and metal atoms.

30. The integrated circuit of claim 25 wherein the spacers have a thickness in the range of about 50 Å to about 500 Å.